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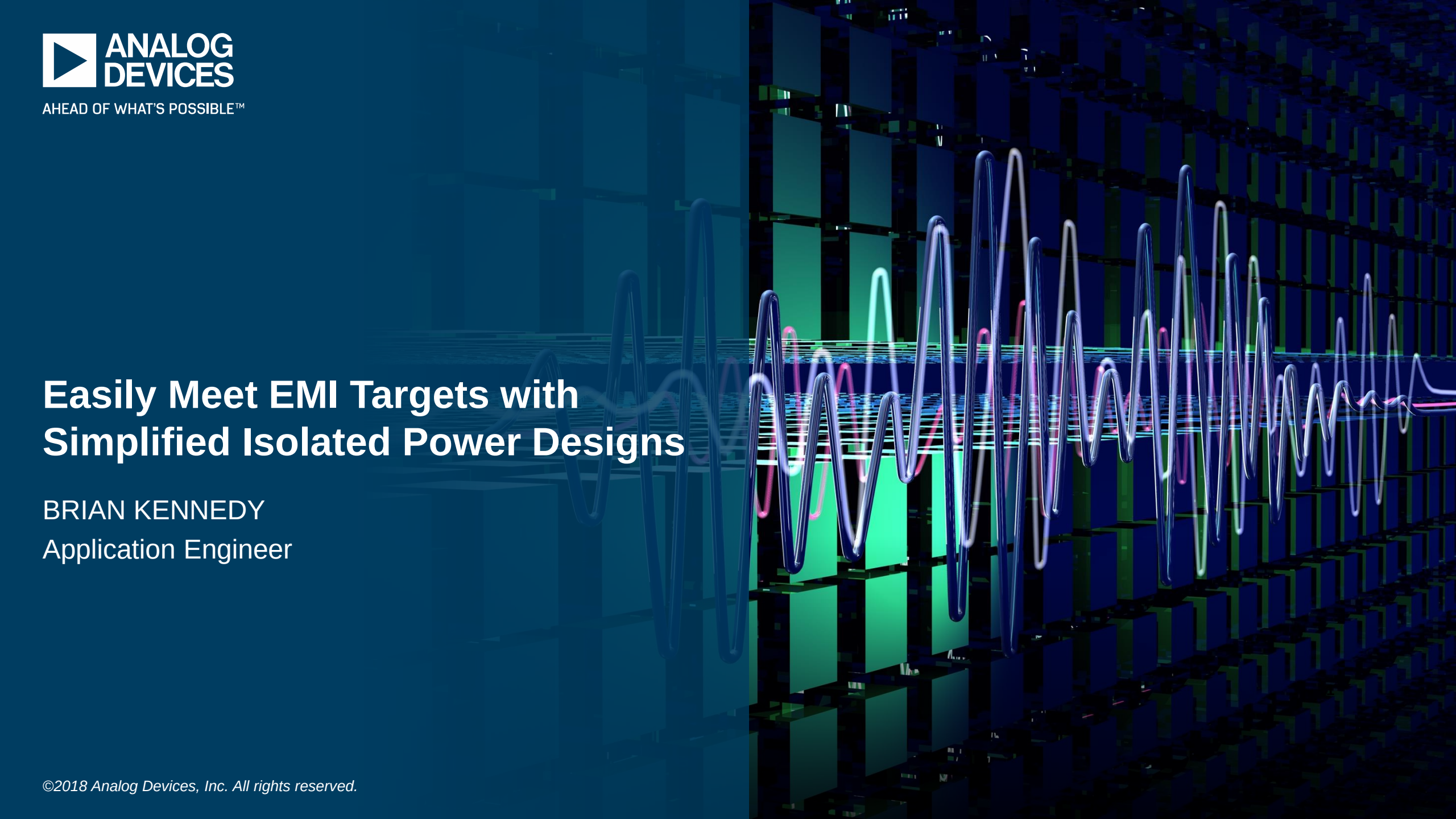

Easily Meet EMI Targets with Simplified Isolated Power Designs

BRIAN KENNEDY

Application Engineer

Presenter

Brian Kennedy

Applications Engineer

Analog Devices Isolation Products

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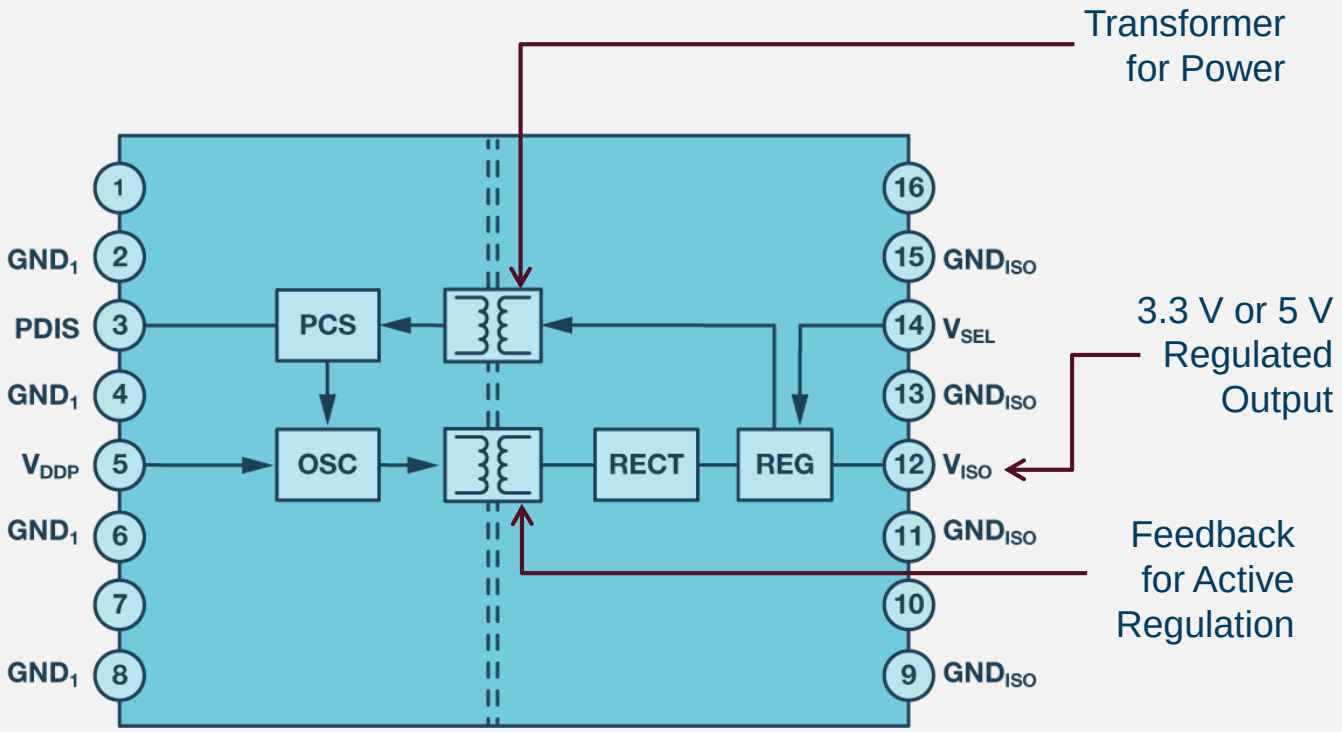
Agenda

- Isolation landscape—integrated power
- The EMI challenge and current methods to solve it
- The need for a new approach
- Next-generation *iso*Power® technology overview
- EMI testing best practices
- Demo: test results
- Next steps
- Q&A

Isolation Landscape: Integrated Power

Small, simplified design for reduced component count



Small 16-Lead Wide-Body SOIC

Analog Devices— first to market **#1**

Advantages

Optimized solutions—no need to design a power supply

Reduced size—with small component count

Innovation—space constrained applications can pack more isolated supplies in a small system

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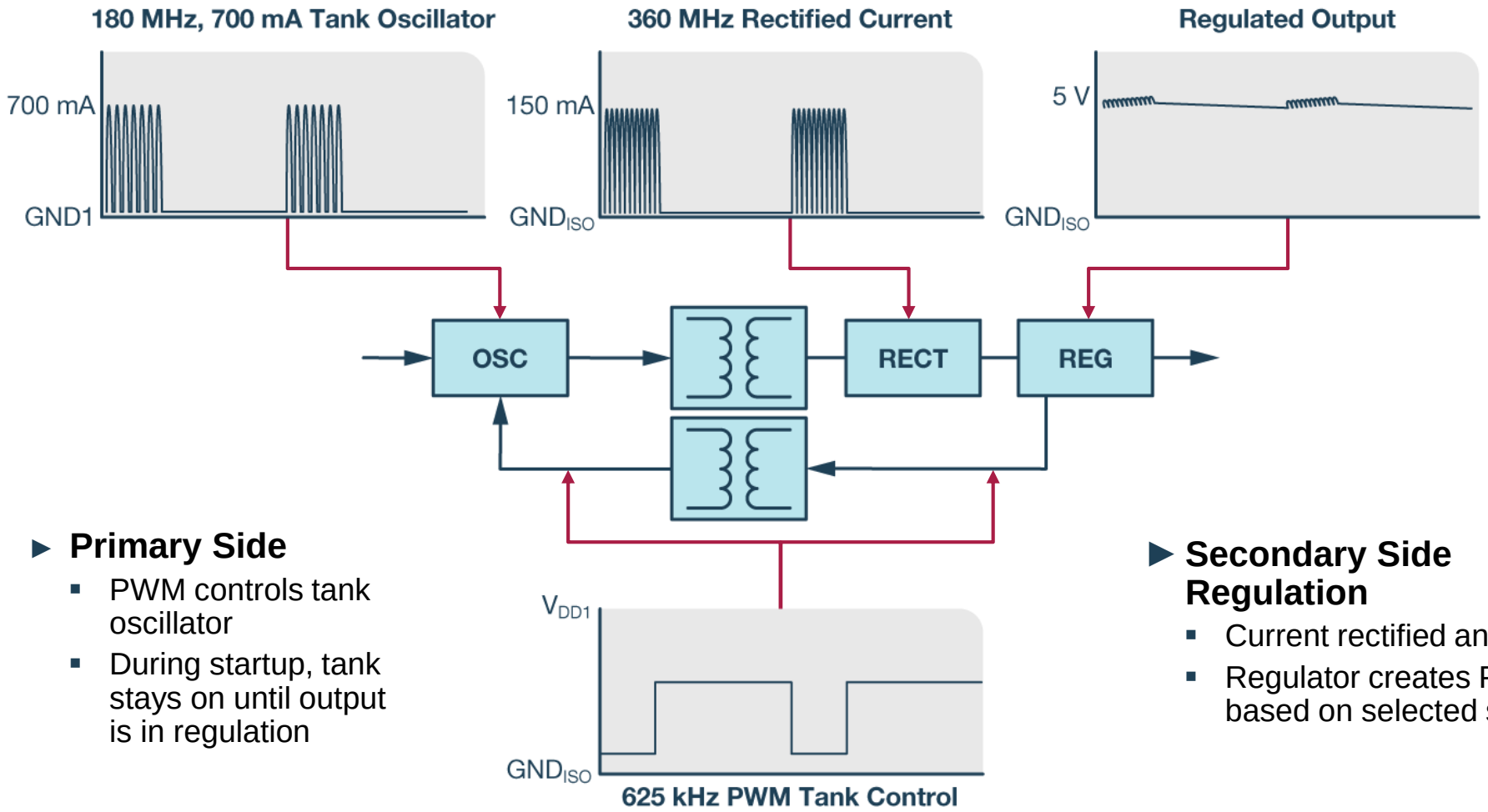
Isolated Power Technology: How It Works

High frequency operation for small size of transformer coils

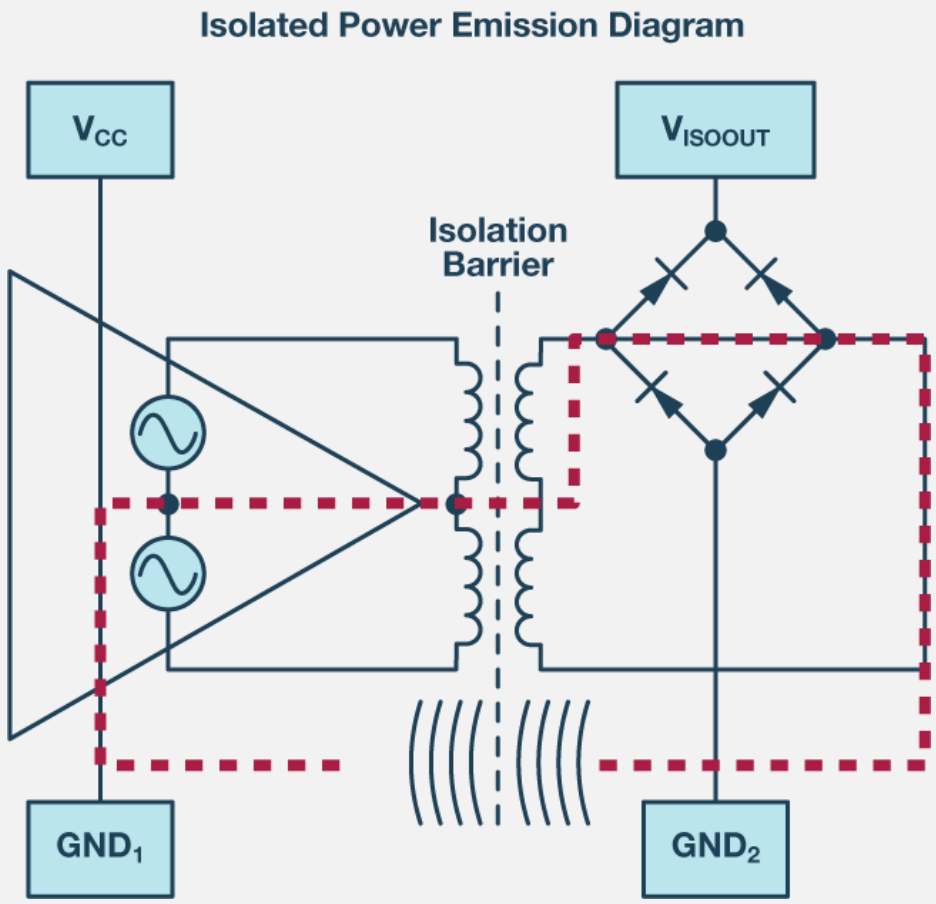


- **Primary Side**
  - PWM controls tank oscillator
  - During startup, tank stays on until output is in regulation

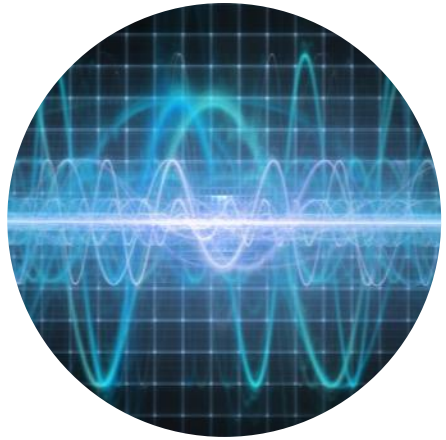
- **Secondary Side Regulation**
  - Current rectified and filtered
  - Regulator creates PWM based on selected set point

The Challenge: Increased Radiated Emissions

- Using 50 MHz to 200 MHz frequencies to obtain small transformer size comes with increased radiated emissions
  - **Common-Mode Current**: Parasitic currents are coupled through the transformer to the secondary side
  - **No Return Path:** No physical path across the isolation barrier for these currents to return creates a dipole antenna that can radiate
  - **Loop Area:** $V_{ISO\ OUT}$ and GND_2 pins connected to planes increase the loop area and the emissions
  - **Stitch Capacitance:** To reduce the dipole emissions, a low impedance return path for the high frequency common-mode currents is needed



The Problem with EMI

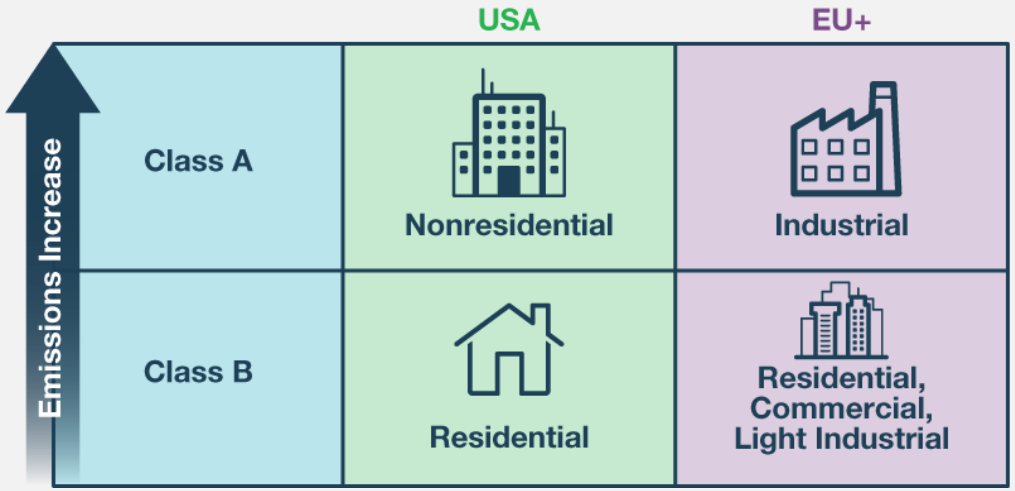


- EMI issues
  - Regulatory compliance
  - RF spectrum pollution
  - Compatibility within circuits
  - System disturbance or malfunction
  - Damage and liability

- Designing for compliance can have a steep learning curve
  - Components
  - PCB (printed circuit board) layout and I/O (input/output)
  - Cables
  - Enclosure and shielding
  - Software and firmware

~50% of designs fail EMI tests the first time

Source: Intertek



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Current Solutions: Mitigate EMI at the Board Level

Tackling emissions **at the board/applications level**, various methods can be effective, but may be difficult or costly to implement

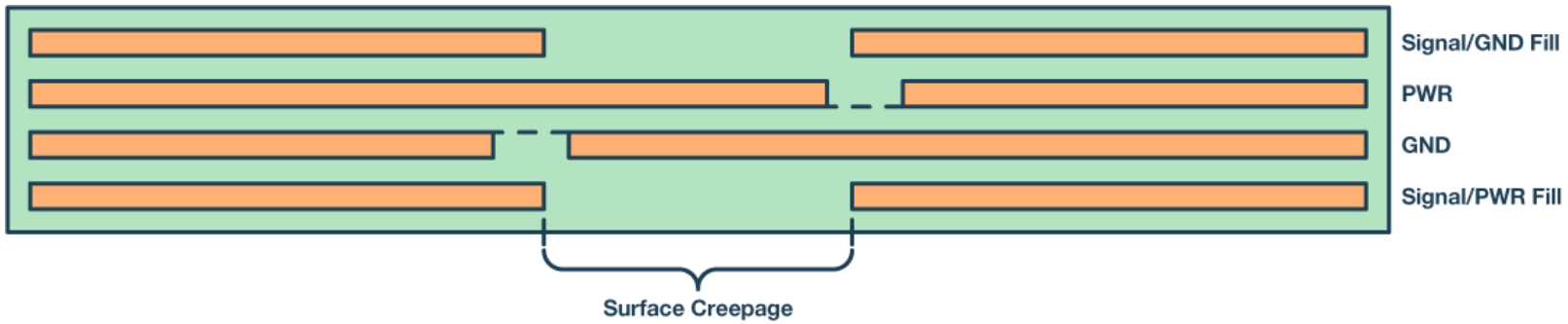
Solution
Stitching Capacitance

Discrete Stitching Capacitor

Disadvantages
Multiple layers, more cost
Difficult to lay out
Increased design/test time
Adds unwanted leakage current

Large and expensive

Overlap Stitching Capacitor for Multilayer PCB
2 Layers of Power plus 2 Layers of Signal



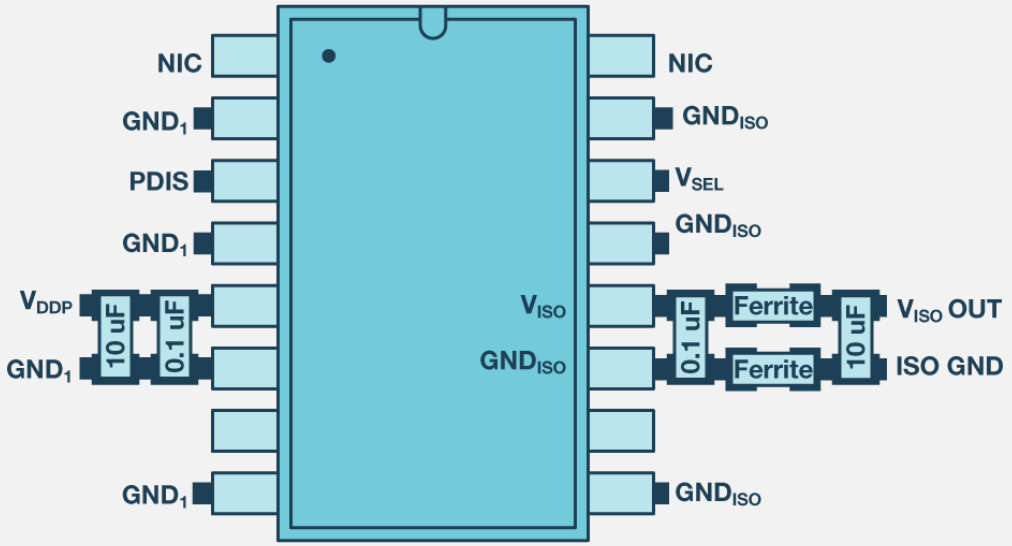
High Voltage Discrete Stitching Capacitor

The Need for a New Solution: Component Level Low Radiated Emissions

- We need a solution **at the component level** that avoids generating high emissions
  - Improved coil design and coil driver circuits
  - Spectrum techniques to reduce the quasi-peak levels
  - Small inexpensive ferrite beads are used to block the high frequency common-mode currents on the secondary supply connections in order to reduce the dipole emissions further

Capable of passing CISPR 22 Class B emissions standard without the use of stitching capacitance on a 2 layer PCB

The New Isolated Power



The Next-Generation *iso*Power® Family

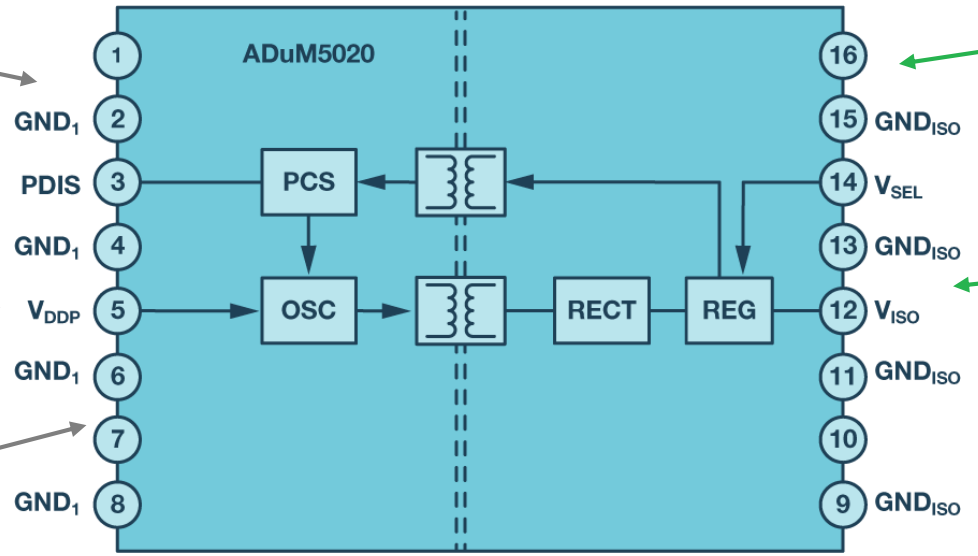
Improved Robustness and EMC

Also Present on ADuM5000

16-Lead SOIC_W Package

3.3 V or 5 V Supply Operation

3.0 kV or 5.0 kV Isolation



Low Radiated Emissions: Isolated DC-to-DC Converter Meets CISPR 22 Class B

Expanded Temperature Range to 125°C

Smallest Package Option 8-Lead SOIC_IC

Use a 2 Layer PCB and Meet CISPR 22 Class B

	Output Power	Isolation Rating	Package
ADuM5028	0.3 W	3 kV rms	8-lead SOIC_IC
ADuM6028	0.3 W	5 kV rms	8-lead SOIC_IC
ADuM5020	0.5 W	3 kV rms	16-lead SOIC_W
ADuM6020	0.5 W	5 kV rms	16-lead SOIC_IC

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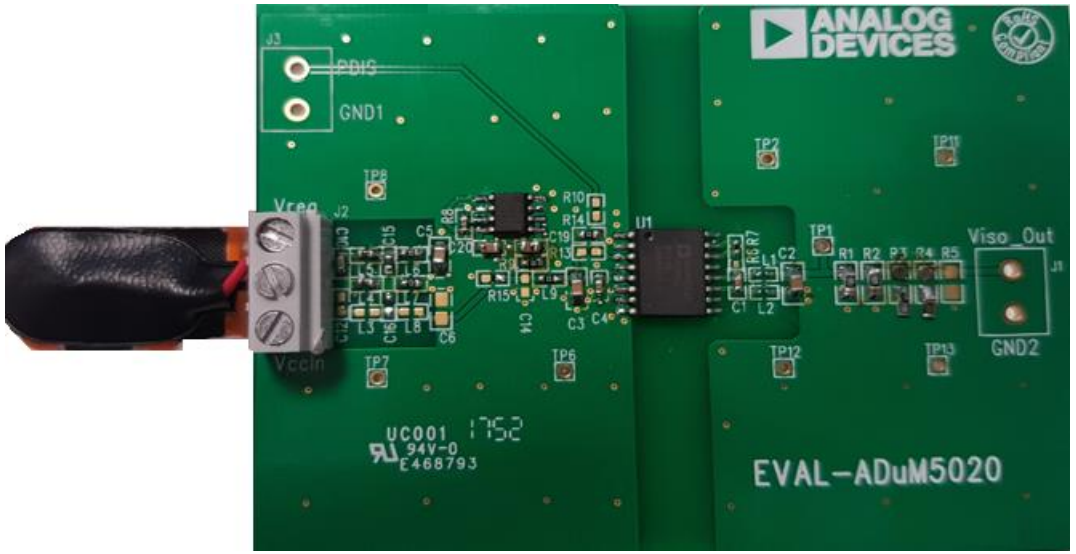
EMI Test Setup

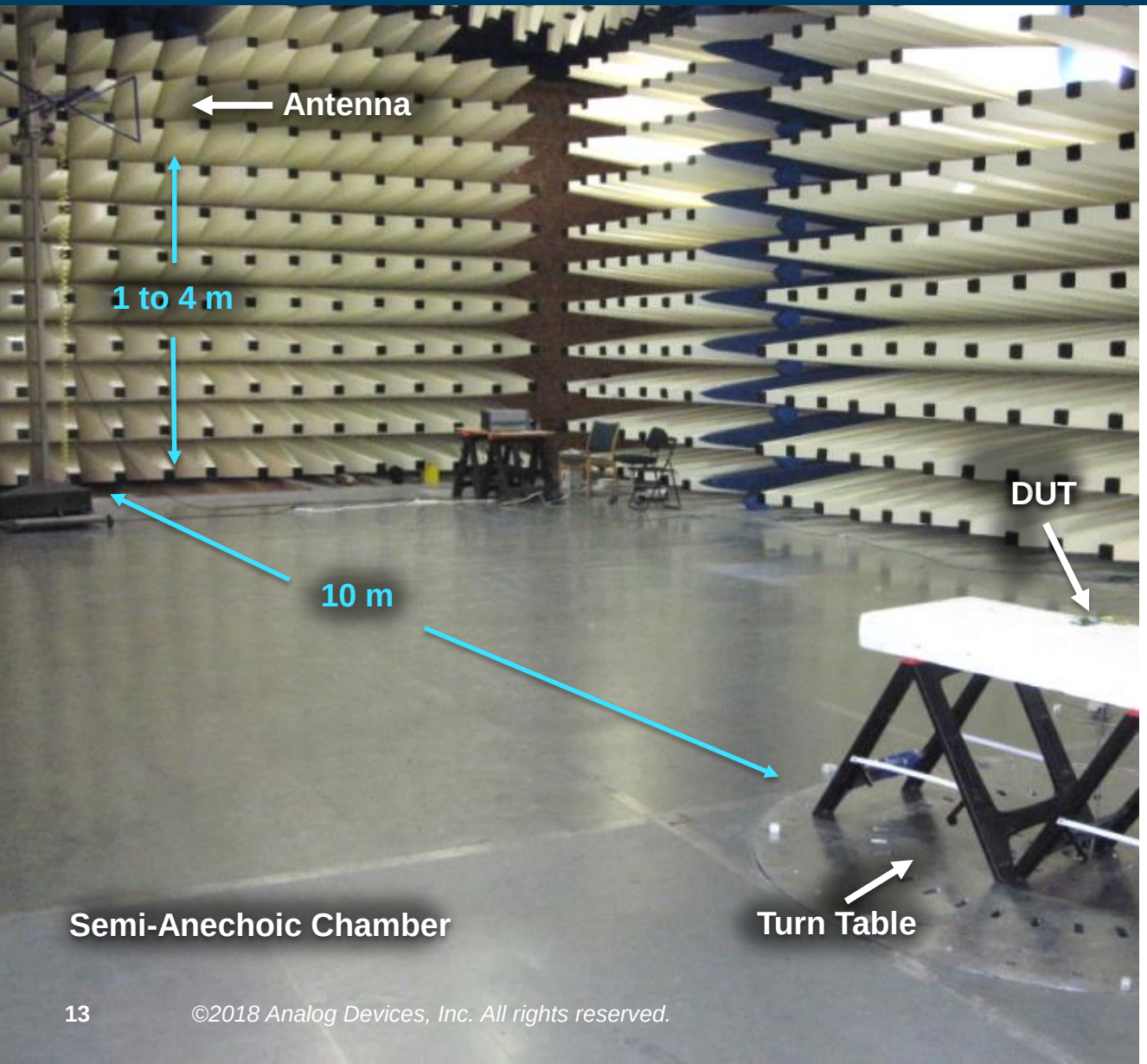
EMI Testing Best Practices

- Reduce the system-level effects in emissions testing
  - Use a local power source (battery) to keep current loop small
  - Have a low drop out regulator on the PCB to power the IC with a stable source
  - Reduce the size of long PCB traces that can increase the current loop on the source and signal connections to the device under test



Goal is to meet the CISPR 22/ EN 55022 Class B emissions standard:
Information technology equipment—radio disturbance characteristics

Radiated Emissions
CISPR 22/EN 55022—Test Chamber Setup



- **Device under test (DUT)** in semi-anechoic chamber
  - Our evaluation board or
  - Customer board/module
- DUT/PCB on a nonconductive turntable
  - Non-floor standing DUTs must be 0.8 m above the horizontal ground reference plane
- Antenna detects emissions
  - 10 m from DUT
  - 1 m to 4 m height
  - Horizontal or vertical
- Auxiliary equipment placed outside the chamber

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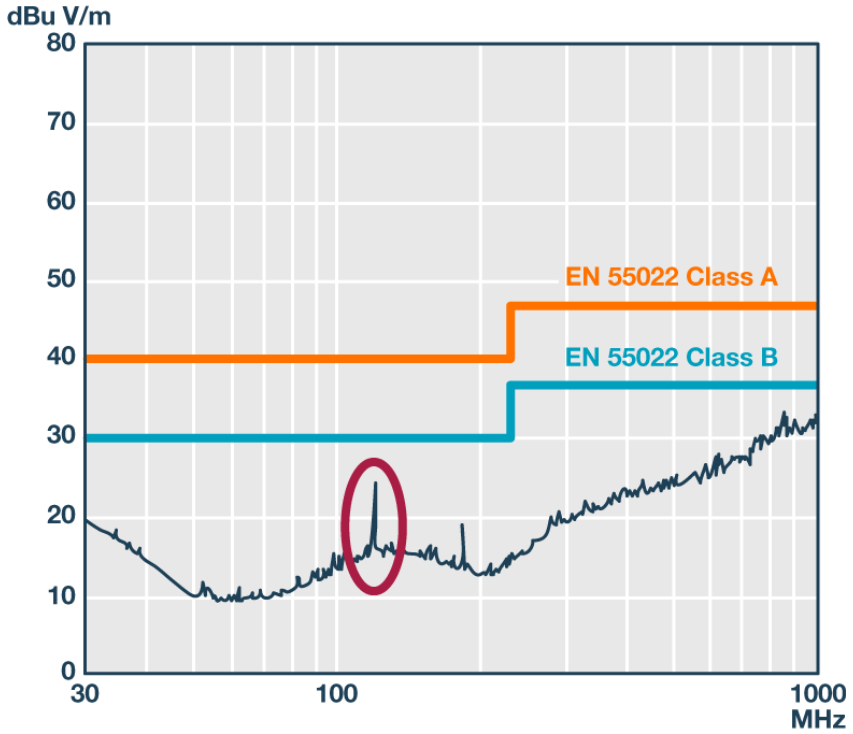
Radiated Emissions
CISPR 22/EN 55022: Test Procedure



EN 55022 Class A and Class B Limits from 30 MHz to 1 GHz

Step 1: Find the peak emissions with a spectrum analyzer

Step 2: Capture quasi-peak measurement

Step 3: Use a full rotation of turntable and vary antenna height from 1 m to 4 m

Step 4: Antenna used in horizontal and vertical orientations

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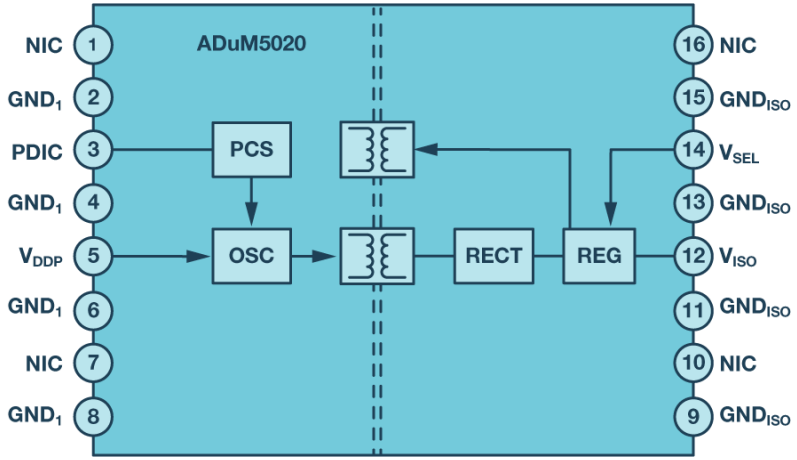
EMI Test Results

Measuring Radiated Emissions with *iso*Power®

ADuM5020

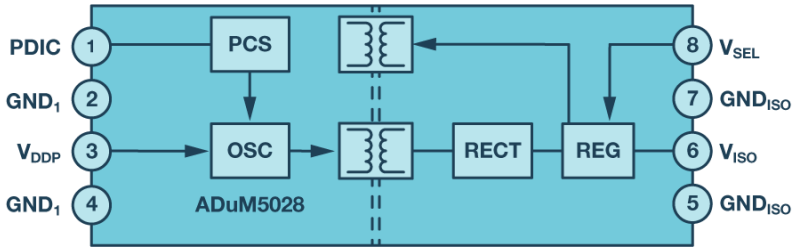


16-lead SOIC_W 100 mA max load

CISPR 22/EN 55022 Class B tests

10 m chamber at CEI, Ireland

ADuM5028



8-lead SOIC_IC 60 mA max load

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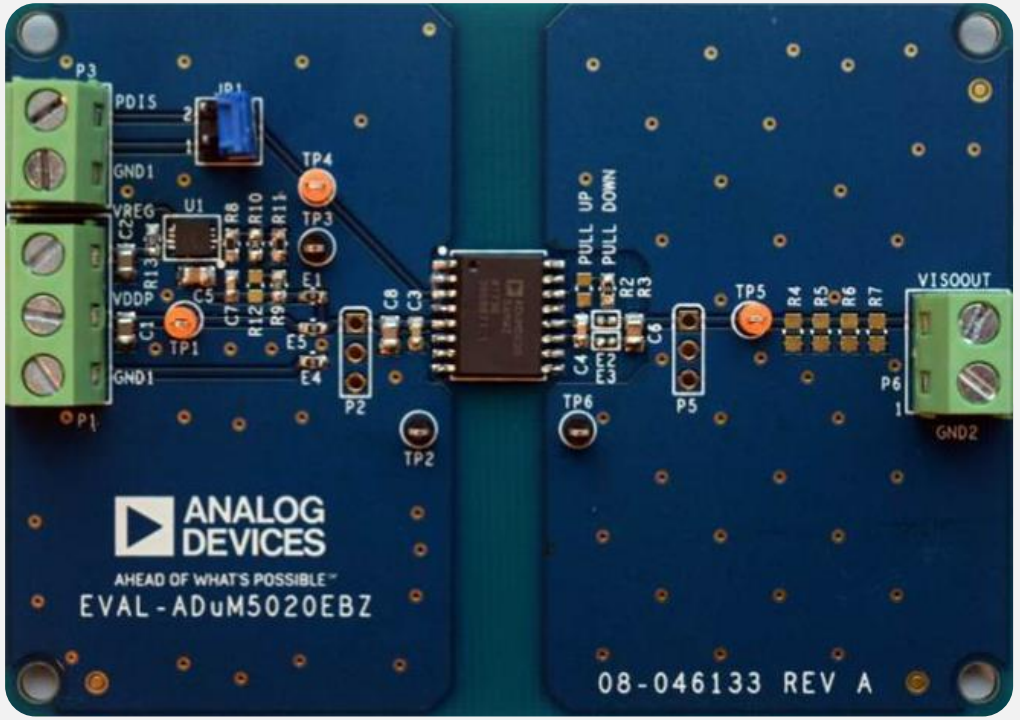
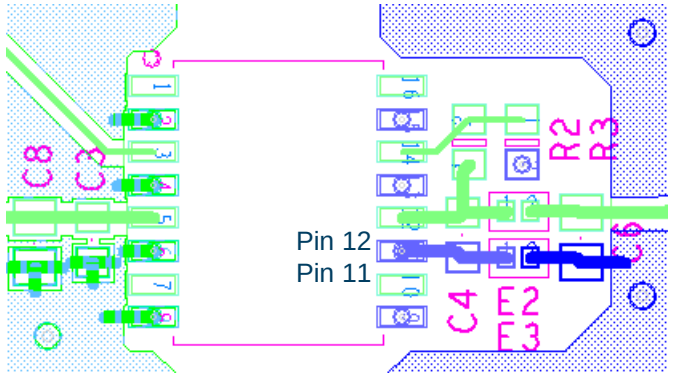
Simplified 2 Layer PC Board Layout

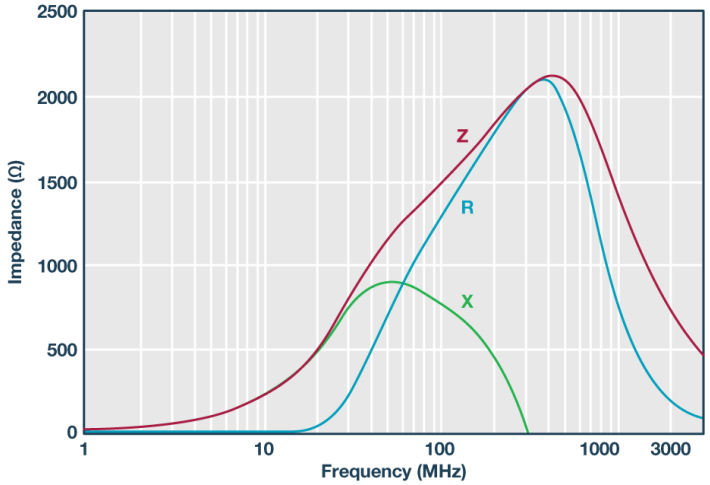
ADuM5020 and **ADuM5028** evaluation boards with 2 layer PCB, meet CISPR 22 Class B using ferrites on V_{ISO} and GND_{ISO}, but without stitching capacitance





Example of ADuM5020 16-lead SOIC Zoomed In on Pin 11 GND_{ISO} and Pin 12 V_{ISO}

Ferrites E2, E3 and Bypass Capacitors C4, C6



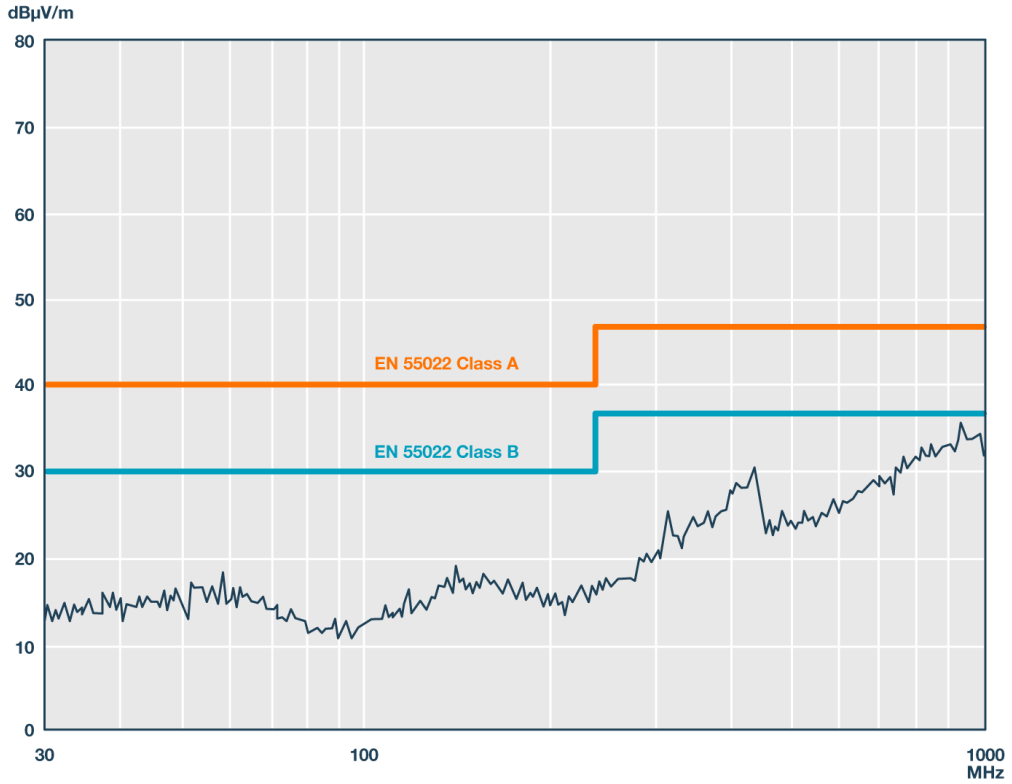
Ferrites E2, E3

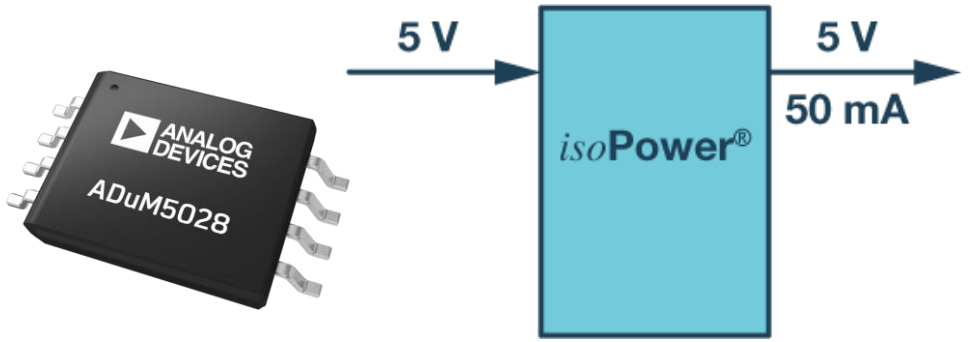
Murata BLM15HD182SN1

Impedance of 1500 Ω at 100 MHz to 1000 MHz

ADuM5028: Meeting CISPR 22 Class B

ADuM5028 with 50 mA Load





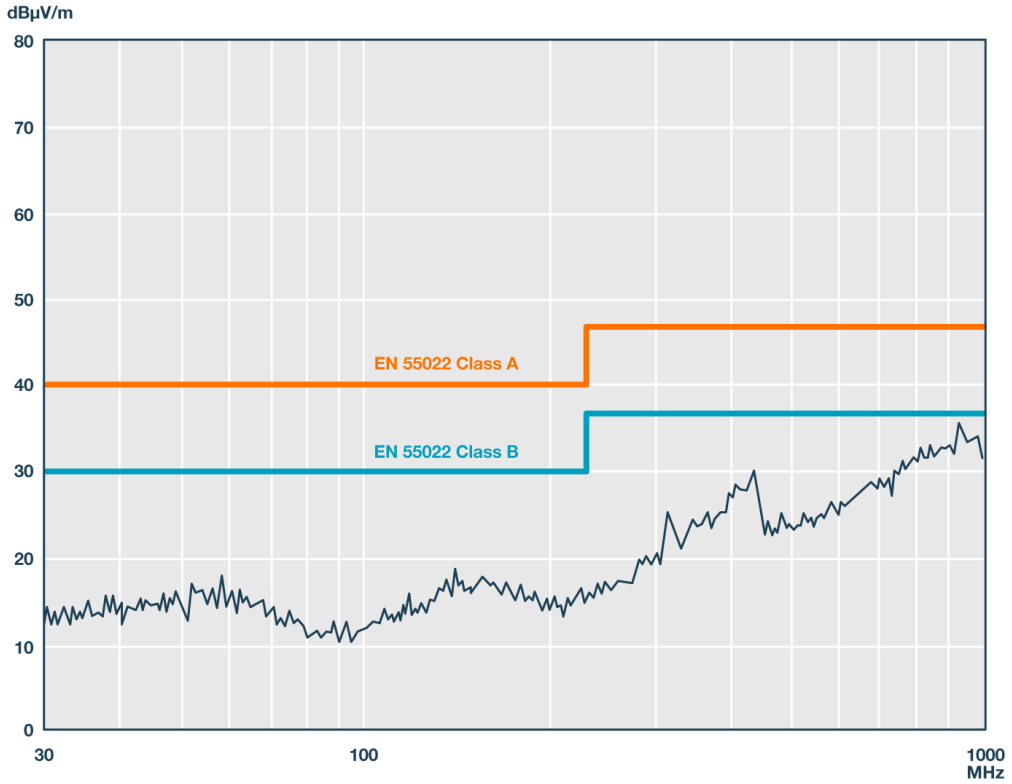
30 MHz to 1000 MHz Results

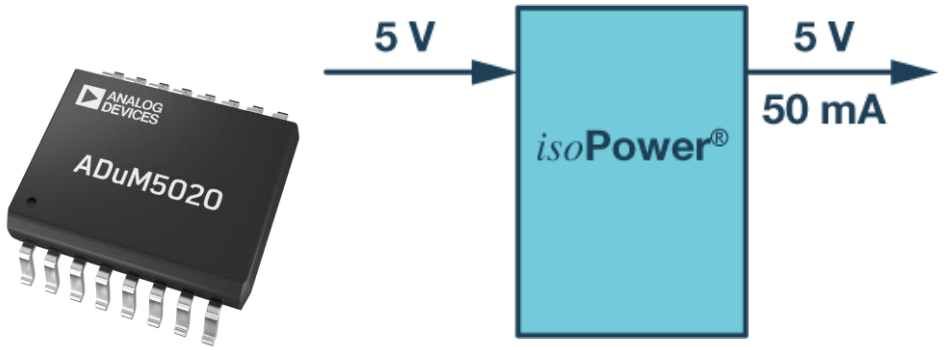
Frequency (MHz)	Angle (°)	Height (m)	Quasi-Peak Measurement (dBµV/m)	Class B Limit (dBµV/m)	Quasi-Peak Margin from Class B Spec (dB)
308.9	180	3.5	25.3	37	–11.7
396.956	0	2	27.7	37	–9.3
428.668	0	2	27	37	–10
920.04	0	1	30.7	37	–6.3

Using 2 Layer PCB: Quasi-peak meets CISPR 22 Class B by –6.3 dBµV margin @ 920 MHz

ADuM5020: Meeting CISPR 22 Class B

ADuM5020 with 50 mA Load





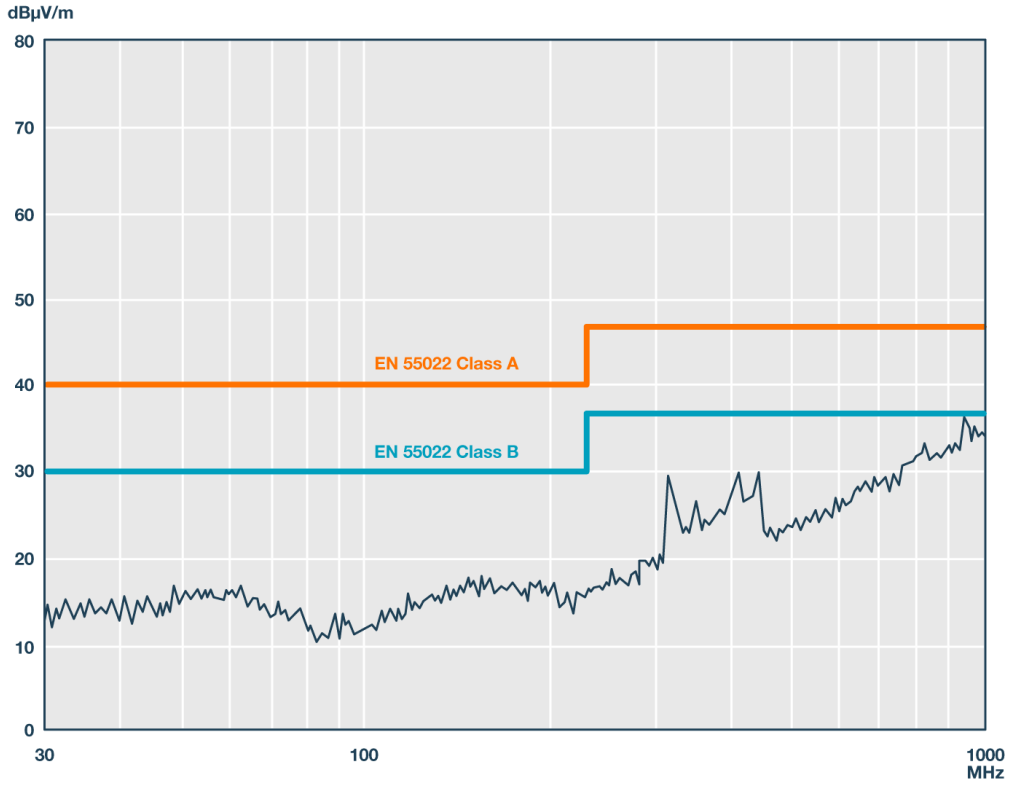
30 MHz to 1000 MHz Results

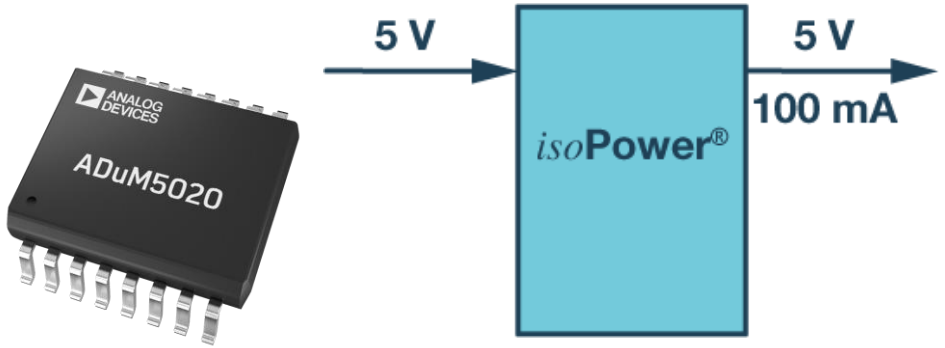
Frequency (MHz)	Angle (°)	Height (m)	Quasi-Peak Measurement (dBµV/m)	Class B Limit (dBµV/m)	Quasi-Peak Margin from Class B Spec (dB)
310.2	180	3	24.1	37	–12.9
426.256	0	3	26.7	37	–10.3
359.004	180	1	23.7	37	–13.3
935.76	0	1	30.1	37	–6.9

Using 2 Layer PCB: Quasi-peak meets CISPR 22 Class B by –6.9 dBµV margin @ 935 MHz

ADuM5020: Meeting CISPR 22 Class B with 100 mA Load

ADuM5020 with 100 mA Load





30 MHz to 1000 MHz Results

Frequency (MHz)	Angle (°)	Height (m)	Quasi-Peak Measurement (dBµV/m)	Class B Limit (dBµV/m)	Quasi-Peak Margin from Class B Spec (dB)
305.656	180	3	28.3	37	–8.7
336.892	180	2.5	27.3	37	–9.7
396.532	180	2	28.5	37	–8.5
426.456	180	2	25.3	37	–11.7
915.264	0	1	31.9	37	–5.1

Using 2 Layer PCB at 100mA : Quasi-peak meets CISPR 22 Class B by –5.1 dBµV margin @ 915 MHz

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Expected Benefits and Next Steps

Emissions Results

Analog Devices new **ADuM5028** and **ADuM5020** meet CISPR 22 class B on a **2 layer PC board with ferrites on V_{ISO} and GND_{ISO} and without the use of stitching capacitance**:

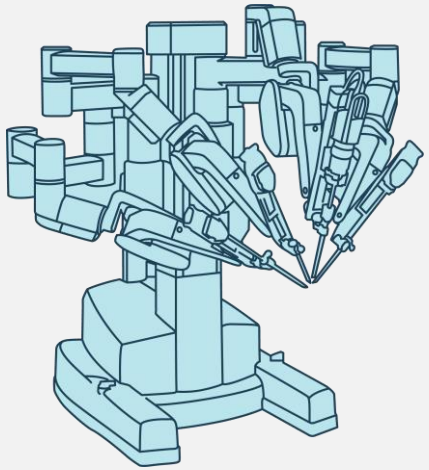
V_{IN}/V_{ISO} 5 V/5 V	V_{ISO} Output Current (mA)	Worst-Case Quasi-Peak Frequency (MHZ)	CISPR 22 Class B Quasi-Peak dBµV/m Class B Margin (dB)
ADuM5028	50	920	Passes by −6.3
ADuM5020	50	935	Passes by −6.9
ADuM5020	100	915	Passes by −5.1

Benefits of the New *iso*Power®

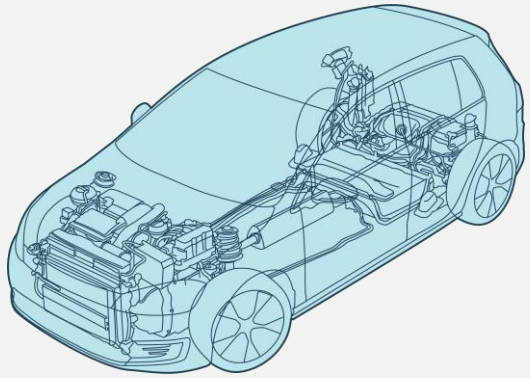
Build Safe and Low Noise Applications with Simplified Certification Process

- Regulatory compliance—meet the CISPR 22/ EN 55022 Class B standard the first time
- Reduced complexity—no stitching capacitance needed
- Faster time to market—reduced PCB design and test time
- Smallest solution size—up to 70% space savings
- Lower material cost—30% cost savings with 2 layer PCB board

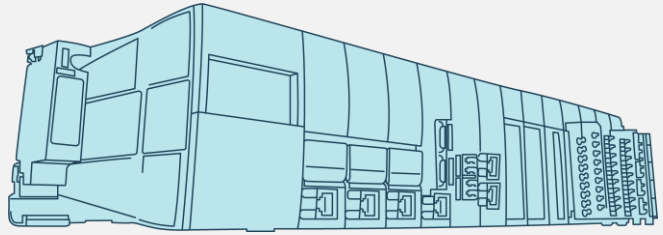
Small, High Density, High Voltage Emerging Applications



Surgical Robot



HEV/EV Vehicles



Programmable Logic Controller (PLC)

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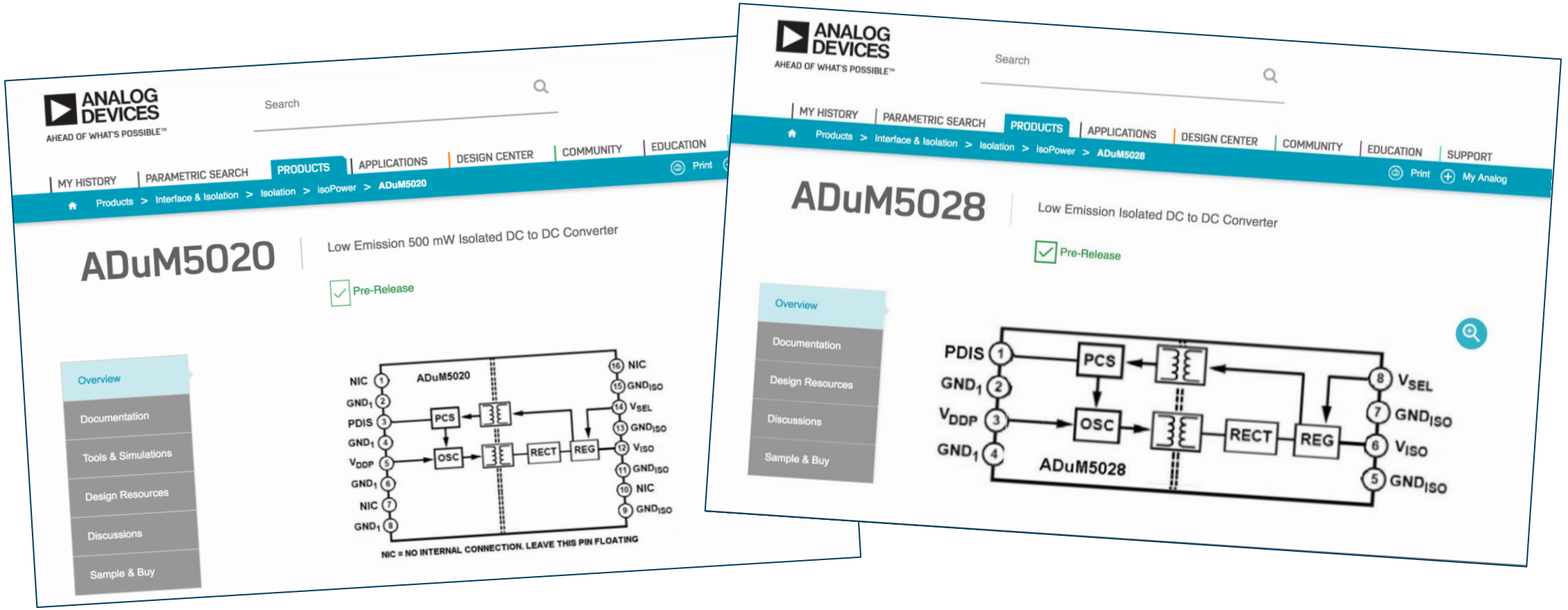
Next Steps with *iso*Power®

Visit analog.com/ADuM5020 and analog.com/ADuM5028 for more resources

Order an eval board EVAL-ADuM5020EBZ or EVAL-ADuM5028EBZ with user guide containing layout and emissions data



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